Amendments to the Specification

Please replace the Title with the following new Title:

SEMICONDUCTOR DEVICE HAVING A BOOSTING CIRCUIT

TO SUPPRESS CURRENT CONSUMPTION

Please replace the paragraph beginning on page 7, line 25 with the following amended paragraph:

The second detection circuit 15 inputs the output voltage Vpp of the charge pump circuit 11. The second detection circuit 15 also inputs the output Vdet1 of the first detection circuit 13, and is activated when the output Vdet1 of the first detection circuit 13 is at "High" level. The second detection circuit 15 [[13]]outputs a signal at "High" level, when the detected voltage Vpp is lower than the target voltage Vpptarget and the output Vdet1 of the first detection circuit 13 is at "High" level.

Please replace the paragraph beginning on page 9, line 4 with the following amended paragraph:

On the other hand, even though the internal power supply voltage Vpp is lower than the target value Vpptarget [[Vpp]], the second detection circuit 15 outputs a signal at "Low" during a period in which the output Vdet1 of the first detection circuit 13 is not at "High", i.e., before the response time Tres1d has elapsed. Therefore, the pump enable signal in the charge pump circuit 11 is still at "Low" level, and the charge pump circuit 11 is not activated.

Please replace the paragraph beginning on page 11, line 17 with the following amended paragraph:

As described above, in the boosting circuit according to this embodiment, two internal power supply detection circuits for outputting signals for activating a charge pump circuit are arranged, the second detection circuit is activated [[on]] based on an output of the first detection circuit, and the activation/inactivation of the charge pump circuit is controlled based on the output of the second detection circuit. In this manner, since the operation time of the charge pump circuit can be shortened, a current consumption in a standby state can be reduced, and an excessive increase in internal power supply voltage can be suppressed to reduce an amount of ripple included in the internal power supply voltage.

Please replace the paragraph beginning on page 12, line 23 with the following amended paragraph:

~~Durign~~ During a period in which the internal power supply voltage Vpp is higher than a target voltage Vpptarget, both the first and second detection circuits 13 and 15 output signals at "Low" level. When the internal power supply voltage Vpp gradually decreases and becomes lower than the target value Vpptarget [[Vpp]], the output Vdet1 of the first detection circuit 13 becomes "High" after the response time Tres1d elapses.